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## **REMARKS**

Applicant is submitting this amendment to correct typographical errors found in the specification and drawings.

## **Drawings**

A replacement FIG. 1A is attached, replacing  $\Delta \gamma$  with  $\Delta Y$ ,  $\Delta \gamma_1$  with  $\Delta Y_1$  and  $\Delta \gamma_2$  with  $\Delta Y_2$ .

A replacement FIG. 3 is attached, adding reference numeral "24" to DELAY, replacing reference numeral "24" with reference numeral "26" for LATCH, replacing reference numeral "26" with reference numeral "28" for sine LUT, replacing reference numeral "28" with reference numeral "30" for D/A CONVERTER, replacing reference numeral "30" with reference numeral "32" for NV MEMORY, replacing reference numeral "32" with reference numeral "34" for DATA INPUT REGISTER, replacing reference numeral "34" with reference numeral "36" for AND gate, replacing reference numeral "36" with reference numeral "38" for the higher-order-bit address input, replacing reference numeral "38" with reference numeral "40" for the other higher-order-bit address input, and replacing reference numeral "40" with reference numeral "42" for BIT RATE CONTROLLER.

A replacement FIG. 5B is attached, replacing reference numerals "20-1" through "20-6" with reference numerals "70-1" through "70-6" for the D/A converters.

A replacement FIG. 6 is attached, adding reference numeral "88" to the numerically-controlled oscillator (NCO).

A replacement FIG. 12 is attached. It is clear from the specification that the original FIG. 12 was mistakenly filed in place of the correct replacement FIG. 12. Applicant respectfully submits that replacement FIG. 12 finds support in the

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specification on pages 48-49, paragraphs 110-111, and therefore, does not constitute new matter.

If the Examiner has any questions regarding this application, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,

SIERRA PATENT GROUP, LTD.

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Kenneth D'Alessandro

Reg. No.: 29,144

Sierra Patent Group, Ltd. P.O. Box 6149 Stateline, NV 89449 (775) 586-9500 (775) 586-9550 Fax